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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/404,891	09/24/1999	PAUL H. SCOTT	0325.00273	8875

21363 7590 12/08/2004

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EXAMINER	
BURD, KEVIN MICHAEL	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 12/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/404,891	SCOTT ET AL.
	Examiner	Art Unit
	Kevin M. Burd	2631

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *23* is/are allowed.

6)☒ Claim(s) *1-3,9-12,17-22* is/are rejected.

7)☒ Claim(s) *4-8 and 13-16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. This office action, in response to the amendment filed 7/19/2004, is a final office action.

Response to Arguments

2. Applicant is correct in that the previous rejection of the claims was made as being anticipated by the instant application's disclosed prior art (specifically figure 1) and not Mori et al (US 4,727,541). The Examiner apologizes for any confusion this typo on the previous office action may have caused.

3. Applicant's arguments filed 7/19/2004 have been fully considered but they are not persuasive. As stated in the previous office action, the instant application's disclosed prior art "discloses a first circuit configured to present a parallel output data signal from serializer 20 in response to two or more serial data signals that are input to selectable Mux 24 and a first clock signal output from RXPLL 22 and input to deserializer 20. This clock signal will have some phase. The phase of the clock signal will be selected by the RXPLL before outputting the clock signal." It is inherent that a clock signal will have an initial phase. A new different phase will be selected by the PLL according to certain criteria such as adjustments done in the PLL. Applicant states such an interpretation is overbroad and the interpretation is so broad that circuitry 110 and 112 in figure 2 of the specification is not given any weight. The examiner disagrees. As indicated in the previous office action, claims 4-8 and 13-16 were indicated as allowable subject matter. Claim 4 appears to claim the circuitry 110 and 112 of figure 2. For this

reason and the reasons stated in the previous office action, the rejections of the claims are maintained.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 1-3, 9-12, 21 and 22 are rejected under 35 U.S.C. 102(a) as being anticipated by instant application's disclosed prior art (specifically figure 1).

Regarding claims 1 and 9, figure 1 discloses a first circuit configured to present a parallel output data signal from serializer 20 in response to two or more serial data signals that are input to selectable Mux 24 and a first clock signal output from RXPLL 22 and input to deserializer 20. This clock signal will have some phase. The phase of the clock signal will be selected by the RXPLL before outputting the clock signal. The RXPLL 22 recovers the first clock signal from the incoming serial data and presents the serial data and the recovered clock to the inputs 26 and 28 of the deserializer circuit 20 (page 3, lines 1-4). A second circuit is configured to present two or more serial data signals from switchable demux 46. The serial signals are sent to the receive circuit 12 (page 1, lines 16-17) and thereby presenting the first clock signal. These outputs are in response to a second clock signal generated by elements 40 and 42 and parallel input

data input to serializer 44. The clock signal is capable of containing multiple phases and is therefore a "multi-phased clock signal".

Regarding claim 2, the first clock comprises a bit clock. The first clock is generated by using the second clock and the second clock is a bit clock as shown in figure 1 of the instant application.

Regarding claim 3, the second clock comprises a reference clock. REFCLK is input at 56 in figure 1 and is used to generate the bit clock.

Regarding claim 10, figure 1 discloses a first circuit configured to present a parallel output data signal from serializer 20 in response to two or more serial data signals that are input to selectable Mux 24 and a first clock signal output from RXPLL 22 and input to deserializer 20. This clock signal will have some phase. The phase of the clock signal will be selected by the RXPLL before outputting the clock signal. The RXPLL 22 recovers the first clock signal from the incoming serial data and presents the serial data and the recovered clock to the inputs 26 and 28 of the deserializer circuit 20 (page 3, lines 1-4). A second circuit is configured to present two or more serial data signals from switchable demux 46. The serial signals are sent to the receive circuit 12 (page 1, lines 16-17) and thereby presenting the first clock signal. These outputs are in response to a second clock signal generated by elements 40 and 42 and parallel input data that is input to the serializer 44. The clock signals will control the pulse width by dividing the clock in element 40. The clock signal is capable of containing multiple phases and is therefore a "multi-phased clock signal".

Regarding claim 11, the first clock comprises a bit clock. The first clock is generated by using the second clock and the second clock is a bit clock as shown in figure 1 of the instant application.

Regarding claim 12, the second clock comprises a reference clock. REFCLK is input at 56 in figure 1 and is used to generate the bit clock.

Regarding claim 21, the first clock signal will have some phase. The phase of the clock signal will be selected by the RXPLL before outputting the clock signal. This circuit comprises a phase selection circuit

Regarding claim 22, the first clock signal will have some phase. The phase of the clock signal will be selected by the RXPLL before outputting the clock signal. This circuit comprises a phase selection circuit. Numerous phases are possible for this clock signal.

Allowable Subject Matter

5. Claim 23 is allowed.

6. Claims 4-8 and 13-16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin M. Burd whose telephone number is (571) 272-3008. The examiner can normally be reached on Monday - Thursday 9 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kevin M. Burd
12/6/2004

KEVIN BURD
PRIMARY EXAMINER